

Claims

What is claimed is:

- 1 1. A structure for implementing an integrated conductor and
2 capacitor in a surface mounted device (SMD) package comprising:
3 a first pair of contacts contained within the SMD package for mating
4 engagement with a first pair of corresponding SMD package contacts;
5 a second pair of contacts contained within the SMD package for
6 mating engagement with a second pair of corresponding SMD package
7 contacts;
8 a conductor extending between said first pair of contacts and
9 contained within the SMD package; and
10 a capacitor defined between said second pair of contacts and
11 contained within the SMD package.

- 1 2. A structure for implementing an integrated conductor and
2 capacitor as recited in claim 1 further includes an additional one or pair of
3 integral capacitors for providing additional capacitance to ground to decouple
4 common mode noise from the power planes.

- 1 3. A structure for implementing an integrated conductor and
2 capacitor as recited in claim 2 further includes an additional one or pair of
3 third contacts contained within the SMD package for mating engagement
4 with a corresponding SMD package third contact and wherein said additional
5 one or pair of integral capacitors is defined between a respective one of said
6 third contacts and one of said second pair of contacts and contained within
7 the SMD package.

- 1 4. A structure for implementing an integrated conductor and
2 capacitor as recited in claim 1 wherein said first pair of contacts are outer
3 contacts and said second pair of contacts are inner contacts, located
4 between said first pair of contacts.

1 5. A structure for implementing an integrated conductor and
2 capacitor as recited in claim 4 wherein said conductor is a generally U-
3 shaped member extending between said first pair of contacts and contained
4 within the SMD package.

1 6. A structure for implementing an integrated conductor and
2 capacitor as recited in claim 5 wherein said capacitor includes a pair of posts
3 respectively supported by said second pair of contacts, each post including
4 at least one outwardly extending plate; and said respective plates extending
5 in parallel.

1 7. A structure for implementing an integrated conductor and
2 capacitor as recited in claim 1 includes a dielectric material surrounding said
3 conductor and said capacitor.

1 8. A structure for implementing an integrated conductor and
2 capacitor as recited in claim 7 wherein said dielectric material includes a
3 selected one of the group of dielectric materials including NPO, X7R, X5R,
4 C0G, and YTV.

1 9. A structure for implementing an integrated conductor and
2 capacitor as recited in claim 1 includes a first dielectric material surrounding
3 said conductor and a second dielectric material surrounding said capacitor.

1 10. A structure for implementing an integrated conductor and
2 capacitor as recited in claim 9 wherein said first dielectric material is a
3 dielectric material having selected impedance properties for high speed
4 operation and wherein said second dielectric material includes a selected
5 one of the group of dielectric materials including NPO, X7R, X5R, C0G, and
6 YTV.

1 11. A structure for implementing an integrated conductor and
2 capacitor in a surface mounted device (SMD) package comprising:
3 a first outer pair of contacts contained within the SMD package for
4 mating engagement with a first pair of corresponding SMD package
5 contacts;
6 a second inner pair of contacts contained within the SMD package
7 between said first outer pair of contacts for mating engagement with a
8 second pair of corresponding SMD package contacts;
9 at least one third contact contained within the SMD package between
10 said second inner pair of contacts for mating engagement with a respective
11 corresponding third SMD package contact;
12 a conductor extending between said first pair of contacts and
13 contained within the SMD package;
14 a first capacitor defined between said second pair of contacts and
15 contained within the SMD package; and
16 a second capacitor defined between a respective one of said at least
17 one third contact and one of said second pair of contacts and contained
18 within the SMD package.

1 12. A structure for implementing an integrated conductor and
2 capacitor as recited in claim 11 wherein said conductor is a generally U-
3 shaped member extending between said first pair of contacts and contained
4 within the SMD package.

1 13. A structure for implementing an integrated conductor and
2 capacitor as recited in claim 11 wherein said first capacitor includes a pair of
3 posts respectively supported by said second pair of contacts, each post
4 including at least one outwardly extending plate; and said respective plates
5 extending in parallel.

1 14. A structure for implementing an integrated conductor and
2 capacitor as recited in claim 11 wherein said second capacitor includes at
3 least one of said pair of posts respectively supported by said second pair of
4 contacts including at least one additional spaced apart outwardly extending
5 plate, and a generally L-shaped member supported by one said third contact
6 having a portion extending in parallel with said at least one additional spaced
7 apart outwardly extending plate.

1 15. A structure for implementing an integrated conductor and
2 capacitor as recited in claim 11 includes a dielectric material surrounding
3 said conductor and said first and second capacitors.

1 16. A structure for implementing an integrated conductor and
2 capacitor as recited in claim 15 wherein said dielectric material includes a
3 selected one of the group of dielectric materials including NPO, X7R, X5R,
4 C0G, and YTV.

1 17. A structure for implementing an integrated conductor and
2 capacitor as recited in claim 11 includes a first dielectric material surrounding
3 said conductor and a second dielectric material surrounding said first and
4 second capacitors.

1 18. A structure for implementing an integrated conductor and
2 capacitor as recited in claim 17 wherein said first dielectric material is a
3 dielectric material having selected impedance properties for high speed
4 operation and wherein said second dielectric material includes a selected
5 one of the group of dielectric materials including NPO, X7R, X5R, C0G, and
6 YTV.